IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/821,781
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Appellants.....Stefan Barkaro, *et al.*
Group Art Unit.....2614
Examiner .....Jamal, Alexander
Attorney Docket No. LAN0033US
Title: .....ECHO CANCELING ARRANGEMENT

APPEAL BRIEF

To: COMMISSIONER FOR PATENTS
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Sir:

Pursuant to 37 C.F.R. §41.37, Appellants hereby submit a second revised Appeal Brief for Application No. 10/821,781, filed April 9, 2004. This second revised Appeal Brief is being sent pursuant to the Notification of Non-Compliant Appeal Brief that was issued on May 13, 2010.

Appellants respectfully maintain their appeal to the Board of Patent Appeals and Interferences seeking review of the grounds of rejection in the Final Office Action of December 21, 2004.

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REAL PARTY IN INTEREST

The real party in interest in this pending Appeal is the Assignee, Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES

The Appellants are not aware of any other appeals, interferences, or judicial proceedings that will directly affect, be directly affected by, or otherwise have a bearing on the Board's decision to this pending appeal.

STATUS OF CLAIMS

The drawings stand objected to under 37 CFR §1.83(a) for allegedly failing to show every feature of the invention specified in the claims.

All of Claims 1 – 10 stand rejected under:

- 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement; and
- 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

STATUS OF AMENDMENTS

In response to the Final Office Action of December 21, 2009, a Notice of Appeal was filed in the U.S. Patent and Trademark Office on March 18, 2010, and no Amendments were filed.

SUMMARY OF CLAIMED SUBJECT MATTER

This Summary of Claimed Subject Matter is being revised in response to the Notification of Non-Compliant Appeal Brief issued on May 13, 2010. In particular, the Notification alleges that the Brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal. Without acquiescing to the reasoning of the Notification, a revised Summary is provided as follows.

The present application is entitled "Echo Canceling Arrangement." Claims 1 – 10 are pending, of which Claims 1, 3, and 7 are independent. The independent claims are described below by referencing both Fig. 2 and the corresponding description, provided by paragraph numbering, in the pending application as filed in the U.S. Patent and Trademark Office on April 9, 2004.

Independent **Claim 1** pertains to a circuit that has a line driver **3** having output terminals connected to a load **ZL** to supply a transmit signal to the load ([0025]) and a line receiver **2** having input terminals connected to the load **ZL** for simultaneously receiving a receive signal from the load ([0026]). The circuit is able to cancel the transmit signal on the input terminals of the line receiver **2**, by having the output terminals of the line driver **3** connected to the load **ZL** via equal first impedances **ZS** ([0025]), and the input terminals of the line receiver **2** connected to the load **ZL** via equal first resistors **R1** and to respective ones of the line driver output terminals via equal second resistors **R2** ([0027]). The first impedances **ZS** are complex impedances of an impedance value that are much smaller than an impedance value of the load **ZL** ([0028]) so that a

drive/termination impedance of the line driver **3** matches the load impedance **ZL**, and transconductance amplifiers **4, 5** sense the voltage across the first impedances **ZS** and supply corresponding currents to respective ones of the line driver input terminals ([0029]).

Independent **Claim 3** pertains to an echo canceling arrangement that includes a line driver **3** having two inputs and two outputs ([0025]), a load **ZL** coupled with the outputs of the line driver **3** via first and second impedances **ZS** ([0025)], a line receiver **2** having two inputs that are coupled through a network with the load **ZL** and the outputs of the line driver **3** ([0026]) and [0027]), and transconductance amplifiers **4, 5** that have two inputs and an output ([0029]). The inputs of the first transconductance amplifier **4** are coupled with the first impedance **ZS** and its output with the one input of the line driver **3** ([0029]), and the inputs of the second transconductance amplifier **5** are coupled with the second impedance **ZS** and its output with the other input of the line driver **3** ([0029]). The first and second impedances **ZS** are complex impedances of an impedance value that is much smaller than an impedance value of the load **ZL** so that a drive/termination impedance of the line driver **3** matches the load impedance **ZL** ([0028]).

Independent **Claim 7** pertains to an asymmetric digital subscriber line (ADSL) driver receiver circuit that includes an ADSL driver **3** having two inputs and two outputs ([0025]); a load **ZL** coupled with the outputs of the driver **3** via first and second impedances **ZS** ([0025]); an ADSL receiver **2** having two inputs that are coupled through a network with the load and the outputs of the driver

([0026] and [0027]); transconductance amplifiers **4, 5** having two inputs and an output, of which the inputs of the first transconductance amplifier **4** are coupled with the first impedance **ZS** and the output with the one input of the driver **3** ([0029]), and the inputs of the second transconductance amplifier **5** are coupled with the second impedance **ZS** and its output with the other input of the driver **3** ([0029]). The first and second impedances **ZS** are complex impedances of an impedance value that is much smaller than an impedance value of the load **ZL** so that a drive/termination impedance of the line driver **3** matches the load impedance **ZL** ([0028]).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Appellant respectfully requests that the Board review the grounds stated in the Final Office Action of December 21, 2009, which include:

- objecting to the drawings under 37 CFR §1.83(a) for allegedly failing to show every feature of the invention specified in the claims;
- rejecting Claims 1 – 10 under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement; and
- rejecting Claims 1 – 10 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

ARGUMENT

Objection to the drawings under 37 CFR §1.83(a)

The drawings of the present application are objected to under 37 CFR §1.83(a) as, allegedly, failing to show every feature of the invention specified in the claims. In particular, the objection states that, "the means for coupling the claimed 'transmit signal' along with the claimed input terminals receiving the signals from the transductance stages must be shown or the feature(s) canceled from the claim(s)."

However, it is respectfully submitted that there are no such "means" claimed, and therefore no such "means" are needed to be illustrated. In fact, it is respectfully submitted that the objection to the drawings is actually addressing a feature that is not actually recited in any of the presently rejected claims. To that point, Appellants submit that, with respective to transductance amplifiers **4, 5**, independent Claims 1, 3, and 7 recite, in part, a signal flow therethrough *that requires no further structural means*:

> **Claim 1:** transconductance amplifiers are provided to sense the voltage across the first impedances and supply corresponding currents to respective ones of the line driver input terminals
>
> **Claim 3:** wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with the one input of the line driver and the inputs of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the line driver
>
> **Claim 7:** first and second transconductance amplifiers having two inputs and an output, wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with

> the one input of the driver and the inputs of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the driver.

The Appellants further submit, respectfully, that the connection by which signals are transmitted from the out terminals of the respective transductance amplifiers **4, 5** to the input terminal of the line driver **3** is clearly depicted in Fig. 2 of the present application. That is, the drawing fully illustrates the coupling of the respective transductance amplifiers **4, 5** with the respective impedances **ZS** and the outputs thereof to the input of line driver **3**.

Accordingly, it is respectfully submitted that the objection to the drawings under 37 CFR §1.83(a) goes beyond the scope of the rejected claims, and, therefore, the objection should be reversed.

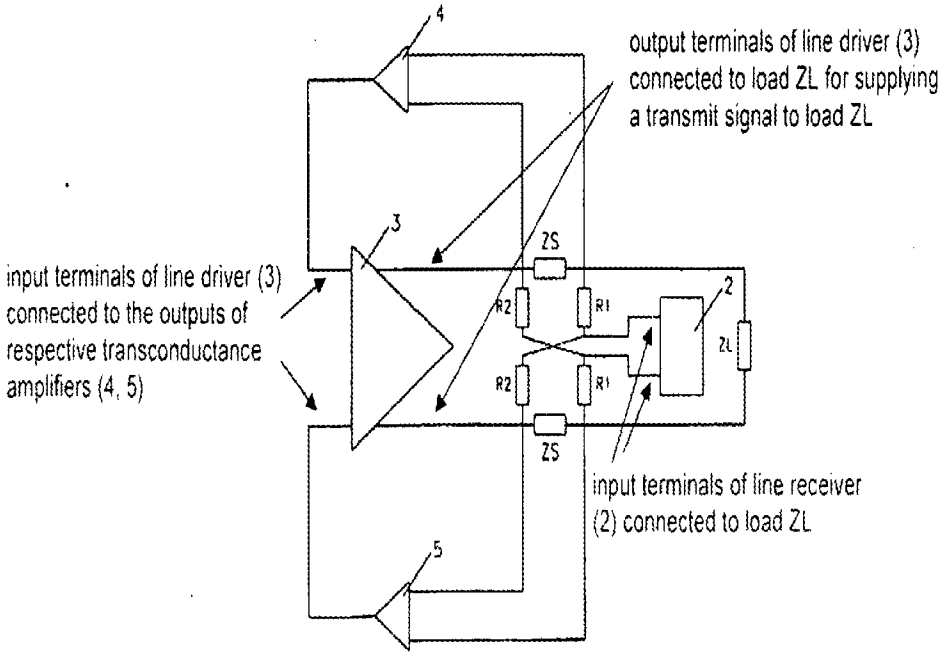
Rejection to Claims 1 - 10 under 35 U.S.C. §112, first paragraph

The Appellants respectfully submit that all of the features of the presently rejected claims, including independent Claims 1, 3, and 7, are sufficiently described, and therefore enabled, by the description in the specification.

It is respectfully submitted that drawings alone *may* be sufficient to provide the "written description of the invention" required by 35 U.S.C. §112, first paragraph (*VasCath inc. v. Mahurkar,* 19 USPQ2d 1111, 1117; 935 F.2d 1555,1565 (Fed. Cir. 1991). Thus, the Appellants provide the following arguments showing where and how the presently claimed features are

sufficiently described, and enabled, in accordance with the specification and drawings, particularly Fig. 2, of the present application.

With regard to **Claim 1**, Fig. 2 of the present application is shown below, with annotations, to show certain features of the rejected claim. Fig. 2 shows a line driver **3** having output terminals connected to a load **ZL** to supply a transmit signal to the load **ZL** and a line receiver **2** having input terminals connected to the load **ZL** to simultaneously receive a received signal from the load **ZL**. Fig. 2 further shows an arrangement, including resistor bridge **R1, R2**, to cancel the transmit signal on the input terminals of the line receiver **2**. The output terminals of the line driver **3** are shown as being connected to the load **ZL** via equal first impedances **ZS** and the input terminals of the line receiver **2** as being connected to the load **ZL** via equal first resistors **R1** and to respective ones of the line driver output terminals via equal second resistors **R2**.



In Fig. 2, the notation "Z" denotes that the first impedances "**ZS**" may be complex, as claimed. At [0028] of the published application, first impedances **ZS** are described as being complex, and it is further described that first impedances **ZS** may be of an impedance value that is much smaller than an impedance value of the load **ZL**, as in Claim 1.

With regard to all of the appealed claims, particularly independent Claims 1, 3, and 7, the rejection states that the claims recite "first impedances which are 'complex impedances to match the load impedance, and are of an impedance value that is much smaller than the impedance value of the load'." The Appellants respectfully submit that the rejection includes an inaccurate characterization of the claimed subject matter. Instead, what is actually recited is:

> **Claim 1:** the first impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance
>
> **Claim 3:** the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance
>
> **Claim 7:** the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance.

That is, **Claim 1** does not recite that the first impedances match the load impedance, but rather recites that the value of the first impedances are much

smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance. The matching described in the specification, therefore, refers to the drive/termination impedance of the line driver, including impedances **ZS**. Accordingly, it is the drive/termination impedance of the line driver that matches the load impedance, as recited in Claim 1, and not the first impedances that match the load as set forth in the rejection.

Further, at [0031] of the application, the drive/termination impedance of the line driver **3** is described as equaling k × **ZS**, whereby "k" is a gain-related function and "**ZS**" is the value of the first impedance. The drive/termination impedance of the line driver, therefore, is a function of both gain and the value of the impedances **ZS**. Thus, the drive/termination impedance of the line driver **3** can be matched to the load when k × **ZS** = **ZL**, as currently recited.

The final rejection further states that, without concrete examples or values or specific implementations, one skilled in the art would not understand the claimed relationship. The Appellants respectfully disagree. In particular, the written description requirement does not demand either examples or actual reduction to practice nor does the requirement demand any particular form of disclosure, *Ariad Pharmaceuticals Inc. v. Eli Lilly & Co.*, 94 USPQ2d 1161, 1172 (Fed. Cir. 2010).

As set forth above, the present application describes the relationship between the different impedances. For example, at [0031], the drive/termination impedance of the line driver equals k × **ZS** and may be matched to the load when

k × **ZS** = **ZL**. Since the relationship between the different impedances is a function of gain of both the line driver **3** and the transconductance amplifiers **4, 5**, as well as the value of the impedances **ZS**, no specific examples or values could make clearer that which is explicitly and unequivocally understandable from the specification. In particular, at [0031], it is stated that any combination of "k" and "**ZS**" that fulfills the equation may be selected, thus implementing a multitude of different gain and impedance values that would permit the drive/termination impedance of the line driver to match the load.

The rejection states, even further, that one of ordinary skill would not be able to determine what the relative size, *i.e.,* "much smaller," would be as recited in Claim 1. In respectfully disagreeing, the Appellants submit that one of ordinary skill would know, by the aforementioned formula from [0031] of the specification, that "much smaller" could easily be approximated by the load impedance **ZL** divided by the gain factor k, *i.e.,* **ZS** = **ZL** ÷ k. That is, "much smaller" is easily determined to be approximately 1/k of the load impedance.

Fig. 2 also shows that the transconductance amplifiers **4, 5** are provided to sense the voltage across the first impedances **ZS** and to supply corresponding currents to respective ones of the line driver input terminals, as claimed. Thus, each feature of Claim 1 is sufficiently illustrated and described in the application to enable one skilled in the art to practice that which is claimed, per the requirements of 35 U.S.C. §112, first paragraph.

With regard to dependent **Claim 2**, which depends from Claim 1, the specification at [0021] describes "a drive/termination impedance of the line driver

may equal the impedance value of one of the impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains," as recited in Claim 1. Once again, the Appellants respectfully submit that there is nothing indeterminate about the impedance relationship recited in Claim 2. It is respectfully submitted, further, that **Claim 6** is similarly supported by the description in the specification of the present application.

Fig. 2 of the present application is shown again below, with annotations, to show certain features of the rejected independent **Claim 3**. Fig. 2 shows a line driver **3** that has two inputs and two outputs, as well as a load **ZL** coupled with the outputs of the line driver **3** via first and second impedances **ZS**, as recited in Claim 3. Further shown is a line receiver **2** that has two inputs coupled through a network, *i.e.,* resistor bridge **R1, R2**, with the load **ZL** and the outputs of the line driver **2**. Further still, Fig. 2 shows first and second transconductance amplifiers **4, 5**, that have two inputs and an output, as recited in Claim 3. The inputs of the first transconductance amplifier **4** are coupled with the first impendence **ZS** and its output is coupled with one input of the line driver **2**, and the inputs of the second transconductance amplifier **5** are coupled with the second impedance **ZS** and its output is coupled with the other input of the line driver **2**, as claimed. The first and second impedances are described as being complex impedances of a value that is much smaller than an impedance value of the load **ZL** so that a drive/termination impedance of the line driver **2** matches the load impedance **ZL**, as claimed, at [0021], [0028], and [0031].

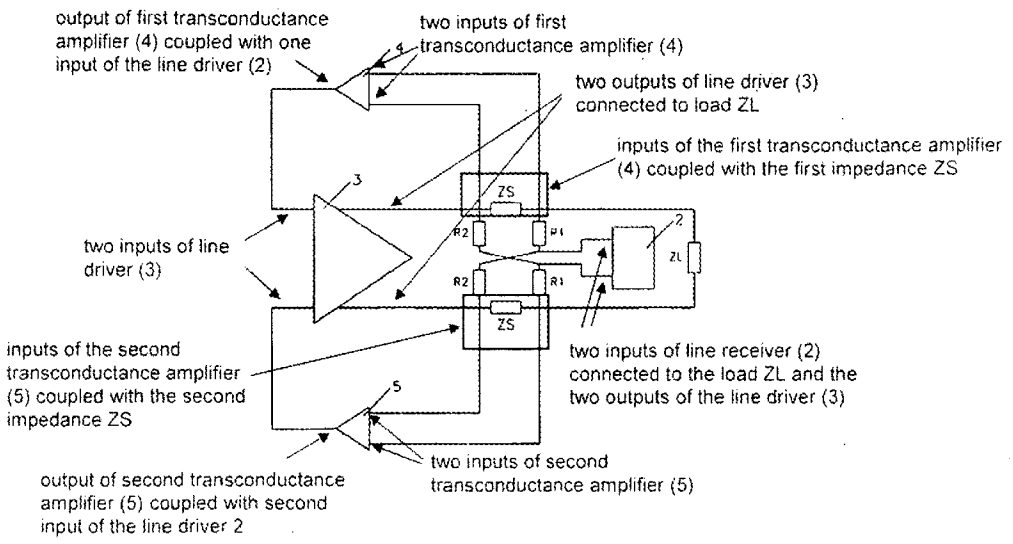
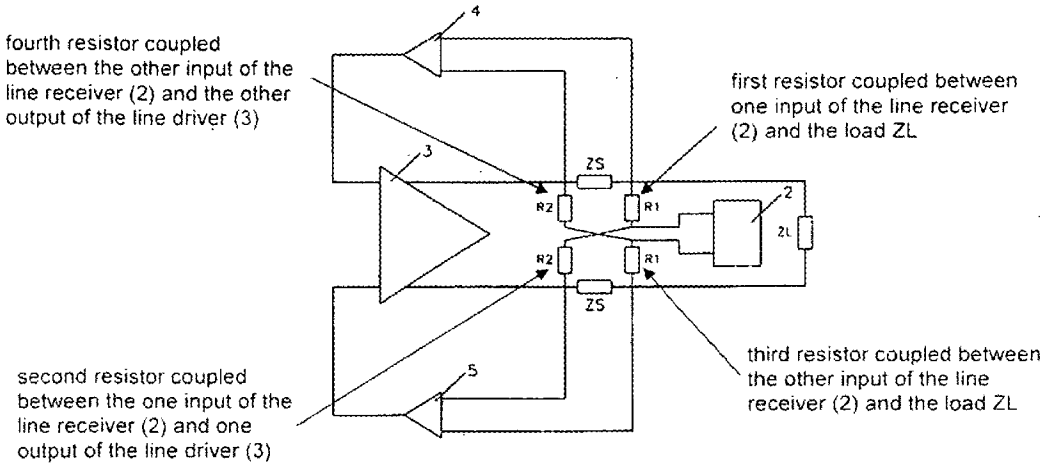


Fig. 2 is again shown, with annotations, to show features of the rejected dependent **Claims 4 and 5**, which depend from Claim 3. Fig. 2 shows a network including a first resistor **R1** coupled between one input of the line receiver **2** and the load **ZL**, and a second resistor **R2** coupled between the one input and the one output of the line driver, as claimed. Fig. 2 also shows a third resistor, *i.e.,* a second instance of **R1**, of the network coupled between the other input of the line receiver and the load and a fourth resistor, *i.e.,* second instance of **R2**, of the network coupled between the other input and the other output of the line driver as in Claim 4.



With regard to **Claim 5**, at [0021] and [0027] of the specification, it is described how the first and third resistors can be equal, and how the second and fourth resistors can also be equal.

It is noted above that **Claim 6** is fully supported by the description for at least the same reasons pertaining to Claim 2.

It is respectfully submitted that **Claims 7 – 10** are substantially similar to Claims 3-6, though the line driver is recited as an "ADSL driver" and the receiver is recited as an "ADSL receiver." Such language is included in the claims as originally filed, and is therefore to be considered part of the original application. Accordingly, Claims 7-10 are sufficiently enabled by the description as originally filed.

For at least the reasons set forth above, it is respectfully submitted that all of the features of the presently rejected claims, including independent Claims 1, 3, and 7, are sufficiently described, and therefore enabled, by the description in the specification. Accordingly, it is requested that the present rejection be reversed.

Rejection to Claims 1 - 10 under 35 U.S.C. §112, second paragraph

The Appellants respectfully submit that all of the features of the presently rejected claims, including independent Claims 1, 3, and 7, are recited in a definitive manner, and therefore the rejection under 35 U.S.C. §112, second paragraph, should be reversed.

In particular, the final rejection asserts that one of ordinary skill would not be able to determine what the relative size, *i.e.,* "much smaller," would be as recited in Claims 1, 3, and 7. In respectfully disagreeing, the Appellants submit that one of ordinary skill would know, by the aforementioned formula from [0031] of the specification, that "much smaller" could easily be approximated by the load impedance **ZL** divided by the gain factor k, *i.e.,* **ZS** = **ZL** ÷ k. That is, "much smaller" is easily determined to be approximately 1/k of the load impedance.

Accordingly, it is respectfully submitted that the claims are recited in a manner that does particularly point out and distinctly claim the subject matter which the applicant regards as the invention, and therefore the present rejection should be reversed.

CLAIMS APPENDIX

1. A circuit comprising a line driver having output terminals connected to a load for supplying a transmit signal to the load and a line receiver having input terminals connected to the load for simultaneously receiving a receive signal from the load, an arrangement for canceling the transmit signal on the input terminals of the line receiver, the output terminals of the line driver being connected to the load via equal first impedances, the input terminals of the line receiver being connected to the load via equal first resistors and to respective ones of the line driver output terminals via equal second resistors, wherein

the first impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance, and

transconductance amplifiers are provided to sense the voltage across the first impedances and supply corresponding currents to respective ones of the line driver input terminals.

2. The circuit according to claim 1, wherein the drive/termination impedance of the line driver equals the impedance value of one of the first impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains.

3. An echo canceling arrangement comprising:

a line driver having two inputs and two outputs,

a load coupled with the outputs of the line driver via first and second impedances,

a line receiver having two inputs, wherein the inputs are coupled through a network with the load and the outputs of said line driver,

first and second transconductance amplifiers having two inputs and an output,

wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with the one input of the line driver and the inputs of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the line driver,

wherein the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance.

4. The echo canceling arrangement according to claim 3, wherein the network comprises:

a first resistor coupled between one input of the line receiver and the load,

a second resistor coupled between the one input and one output of the line driver,

a third resistor coupled between the other input of the line receiver and the load, and

a fourth resistor coupled between the other input and the other output of the line driver.

5. The echo canceling arrangement according to claim 3, wherein the first and third resistors are equal and the second and fourth resistors are equal.

6. The echo canceling arrangement according to claim 3, wherein the drive/termination impedance of the line driver equals the impedance value of one of the first or second impedances multiplied by k, wherein k is a function of the line driver gain and the transconductance amplifier gains.

7. An asymmetric digital subscriber line (ADSL) driver receiver circuit comprising:

an ADSL driver having two inputs and two outputs,

a load coupled with the outputs of the driver via first and second impedances,

an ADSL receiver having two inputs, wherein the inputs are coupled through a network with the load and the outputs of said driver,

first and second transconductance amplifiers having two inputs and an output, wherein the inputs of the first transconductance amplifier are coupled with the first impedance and its output with the one input of the driver and the inputs

of the second transconductance amplifier are coupled with the second impedance and its output with the other input of the driver,

wherein the first and second impedances are complex impedances of an impedance value that is much smaller than an impedance value of the load so that a drive/termination impedance of the line driver matches the load impedance.

8. The circuit according to claim 7, wherein the network comprises:

a first resistor coupled between one input of the receiver and the load,

a second resistor coupled between the one input and one output of the driver,

a third resistor coupled between the other input of the receiver and the load, and

a fourth resistor coupled between the other input and the other output of the driver.

9. The circuit according to claim 7, wherein the first and third resistors are equal and the second and fourth resistors are equal.

10. The circuit according to claim 7, wherein the drive/termination impedance of the driver equals the impedance value of one of the first or second impedances multiplied by k, wherein k is a function of the driver gain and the transconductance amplifier gains.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

CONCLUSION

The Appellants respectfully submit that the evidence of record and the arguments based on such evidence show that the final rejection of the pending claims was in error. In particular, specific grounds for rejection have been identified and reasons have been provided showing that the rejections are not appropriate. The Appellants, therefore, respectfully request that the Board reverse the final rejections for the specific grounds identified herein.

Should any issue remain that prevents furtherance of this Appeal, the Board or Office is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,

SpryIP, LLC

Dated: May 17, 2010

By: /Tim R. Wyckoff/

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